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Ltr	REVISIONS	DATE	INITIALS
A	As Issued	10-75	JOT

Model No.	Stock No.
Title Theory of Operation	
Description	Date
By Brad Reak	Sheet No. 1 of 12
Supersedes	Drawing No. A-5958-4362-9

9320-3246 (6/75)

SERIES 300 DISPLAY COLOR CARD

Theory of Operation

FINAL

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Fort Collins Systems Division

This is the Theory of Operation for the 98545A and 98543A display cards. These cards provide bitmapped color displays for the Series 300 Technical Workstations produced at FSD.

The following documents and specifications are referenced:

TOPCAT ERS describes the operation of the Topcat display controller chip. Document number A-1FH2-2001-7

RODAN Specification describes the low resolution color monitor to be OEM'ed by the Roseville Terminal Division. Document A-35741-90004-1.

JACKPOT Specification describes the low resolution monochrome monitor to be OEM'ed by the Roseville Terminal Division. A-35731-90004-1

DIO Bus specification is the current IO standard for HP's series 200 line of desktop computers.

NEREID ERS describes the operation of the Nereid color mapping display chip. Document number A-1FF3-2001-7.

Allegro specification describes the interface to the High resolution color monitor OEM'ed by FSD. Document number A-1150-9007-1.

FSD Display Rom Definition Describes the FSD standard display board architecture for series 200 computers.

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The Series 300 color board is an upgrade to the low end BOBCAT system with monochrome display. Series 300 color will have four plane color mapping with 8 bit DACs. This allows the user to display 16 colors from a palette of 16,777,216 colors. Buyers have a choice of low resolution or high resolution. The low resolution version displays 512 X 400 pixel pairs and drives the Rodan monitor currently being specified at Roseville Terminal Division. The hi resolution version displays 1024 X 768 individual pixels and uses the Allegro monitor being developed at FSD.

The color card achieves its high level of functionality by making extensive use of LSI. At its heart is the TOPCAT chip. Topcat is an NMOS III chip that provides an integrated bit mapped display with window move hardware and frame buffer support. Color mapping is entirely handled by another NMOS III chip called NEREID. Nereid does the color mapping and D to A conversion. Video memory uses the 4416 nibble wide DRAM.

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3.1 Topcats and Video Ram

The Topcat is the heart of the display board. Topcat can best be described as a Frame Buffer memory manager and window mover. It takes memory data in the on board frame buffer and creates pixel data. This operation is essentially invisible to the rest of the system. To the system, the frame buffer memory appears a normal system ram but organized in a format that makes graphics manipulation easier.

The color board uses the TMS 4416 nibble wide DRAM as described in the TOPCAT ERS. Both high and low resolution boards have four planes of memory. The low res board uses eight memory chips per plane (U_01 to U_08). Hi resolution uses 16 memory chips per plane (U_01 to U_16). Series damping resistors R_01 to R_04 and RP_01 damp the RAM address, RAS and CAS lines. R_05 TO R_07 keep the Topcat DIP port inactive during normal board operation but allow a 3065 board tester to use the DIP port for troubleshooting TOPCATS.

Topcat organizes the framebuffer into an array fixed to 1024 pixels across and either 512,1024 or 2048 lines. It is possible to select the number of displayed lines via programmable Topcat registers. The 98543A card displays 1024 individual pixels across and 400 lines down. This leaves 112 lines of undisplayed frame buffer available for temporary storage of graphics information. Since single horizontal pixels would far exceed the bandwidth of most low cost monitors, it is softwares' responsibility to always use double pixels. The effect is to give horizontal resolution better than 512 pixels without exceeding monitor bandwidth specs. Single pixel snifting is allowed but there must always be at least 2 pixels between adjacent horizontal dots.

The 98545A uses a much higher performance monitor and therefore does not require software to use double pixel algorithms.

3.2 Nereid Color Map

The color board has four plane colormapping. Mapping is entirely under control of the NEREID chip. See the Nereid ERS for particulars on its operation. Since only four planes are used and Nereid supports eight, the top four planes remain unused and

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unavailable.

Due to peculiarities in the Nereid colormap, it is possible to do a write read cycle to Nereid to fast. This is especially true with a combination of fast processor and low resolution display card. The primary reason for this is that the clock is not fast enough to clear Nereids busy bit before another DMO cycle can start.

The error is seen as a bus error timeout at the CPU. The fix is to use a NOP or other delay technique to prevent consecutive Nereid access cycles. Nereid needs at least 16 dot clock cycles between accesses. In the case of the low resolution display (35.904MHz clock) this is 445ns before starting another Nereid access. In the future, faster processors may make this show up on even the Hi resolution card. It is advisable to always check the 16 cycle rule as stated above when writing code for Nereid.

Nereid uses older NMOS technology so therefore requires more than +5V and -2V. U4 is a voltage regulator that supplies Nereid with 6.5V at Vclk and Aclk. Aclk is isolated from Vclk by the lowpass filter L1 and C28. This keeps noise generated by Vclk from coupling directly to the outputs via an internal Nereid path.

1/4 of U2, Q1C and Q8 compose a 3.75V regulator to supply Nereids V1 supply. 1/4 of U2 with Q1A and reference voltage source Q1 supply the -2V needs of Nereid and the res to the board.

Nereid requires a constant current source to establish a reference for the DAC's. This is accomplished using OP amp U2 and the resistor network composed of R4, R6, R11, R12, R13, and R14. The nominal value is 410 microamps into Iref with 1V at the node of R4 and R6.

3.3 Logic Interface to CPU

The internal section of the display card is isolated and buffered from the CPU bus via U10, U15, U21, U26 and U32. The Data buffers U10 and U15 always point from the CPU to the display card unless there is a read request to the board from the processor.

Decoding is accomplished by the custom PAL U19 and decoder U36. U36 with U31 and U38 create a programmable register 3 in the middle of the display ROM address space. A write of any value to register 1 forces the card to reset its interrupts by clearing U38. U37 Returns 0 for unused planes during a read from the frame buffer. Supposedly, this makes software easier to implement.

Topcats used together are very sensitive to anything that may cause them to become unsynchronized. This could happen by doing

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a chip select at a time when individual Topcats may or may not see the select signal. IC's being what they are, some might see the select and some might not. This would cause considerable video distortion. U5 corrects this problem by synchronizing NCS, NSUDS and NSLDS to Topcats clock.

Topcats and Nereids generate their own DTACK and this is fed to the CPU bus thru U14 and U9. Requests to read ROM U20 or write to register 1 or register 3 are DTACKed by walking a 1 thru shift register U18.

The 98545A and 98543A boards will generally conform to DIO specifications, with the following exceptions.

1. Shape factor will be Series 300.

2. Interrupts allow all 7 levels to be programmed via register 3.

3. Edge connector is Series 300 CPU pinout not standard DIO.

4. IMA is generated but not brought to the connector (See U9 pin 8).

3.4 Video Amplifies and Output

Typical video levels seen at the BNC connectors are shown in appendix C. It is important to remember that the video signal rides on a 1.5 volt DC level. The video level is adjusted by pot R6 which controls the current source that supplies Nereids Iref pin.

For the purposes of this explanation, the green amplifier will be explained because the red and blue are similar but without the sync. The transistor Q6 with resistor R80 and R24 form a current to voltage converter that converts the current sink of Nereids output to a voltage that varies from 9.7 volts to 9.0 volts nominal at the base of Q3. The video drive stage is a simple emitter follower that drives the monitor through zener CR3 and the common mode chock T2. T2 serves to prevent a common mode signal from escaping to the outside world and causing RFI problems. Zener CR3 drops a constant 6.8 volts to bring the nominal level no signal level to about 1 volt. Since most monitors use composite sync on green, it is necessary to mix the 0.3 volt sync signal with the video. This is accomplished with the resistor R38 acting to suck out enough current to lower the voltage a the base of Q3 by 0.3 volts during horizontal or vertical sync as controlled by the XOR gate connected to U11. Zener CR9 biases the transistors Q5, Q6, Q7, and Q9 into

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conduction and allows the current to voltage action of the circuit. Zener CR2 biases Q2, Q3 and Q4 and prevents power supply noise from getting into the video.

Any monitor used with the color cards should be AC coupled due to the 1.5 volt bias imposed on the video signal. See appendix C for exact details of the video level and timing.

3.5 Memory Map

Memory configuration conforms to the FSD Display ID ROM Definition. The color boards implementation is shown in appendix A. The Frame buffer and the Topcat register set are fixed in internal address space. The 98545A Topcat registers overlay the Topcat on the 68010 processor board. Deselection of the Topcat on the processor board is accomplished by a switch located on the processor board.

3.6 Interrupt Structure

The interrupt structure is similar to DIO with the exception of being software programmable to all 7 levels. Software must set the interrupt level and turn on interrupts by writing to IE as per DIO. Interrupts are extended DIO by using D3 through D5 at register $560003. Some consistency is obtained with DIO by continuing to use positive logic and by making D3 as the LSB. On receiving an interrupt and verifying the interrupt is coming from the color card, the processor must then poll the Topcat chips to determine the interrupting device.

3.7 Clocks and Timing

The system clock controls the entire timing of the display card. It is based on ECL technology to allow the system to run at a high enough clock rate to drive a Hi resolution monitor. The main oscillator is based on TTL levels and is converted to a ECL level by U35. The actual description of the circuit would be long winded and probably useless to the reader. Instead, you are encouraged to study the timing diagrams with the clock schematic close by. The only peculiar part of the circuit would be the adjustable duty cycle of Dclk2. This is accomplished by using an adjustable RC network composed of R85, R79 and C16. The capacitor is allowed to charge to a level high enough to trigger U27 and is then forced to discharge when Q11 is turning on the the state change of U27. Q11 is made stable by the temperature compensation circuit labeled cbias. Cbias room temperature voltage level should be about -2VDC. U27 is forced to oscillate

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by alternately toggling set and reset as per the timing diagram.

Main clock frequencies will change with the different monitors. Values programmed into Topcat registers are dependent on the value of the system clock. Therefore, software must use the information in the ID/FONT ROM to determine the timing constants for correct initialization of board. Board clock rates and the required Topcat register values are shown in appendix B. When computing values for the Topcat registers, it is important to account for the 12 pixel skew induced by Topcat on the Front Porch and Back Porch. Additionally, there is a 24 pixel delay for Cblank signal as it travels through Nereid and the Sync doesn't. As an example, with the Topcat register values shown below, the real horizontal sync and blanking times are computed as shown:

h1t = C040 = 1024 pixels h2t = 1008 = 128 pixels h3t = A007 = 112 pixels h4t = 7009 = 144 pixels

Front Porch = (128 -12 -24)pixels = 92 pixels

Back Porch = (144 + 12 + 24)pixels = 180 pixels

Assume a 35.904 MHz clock. Then a pixel is equal to 1/35.904MHz or 27.85ns. The actual Front Porch and Back Porch can then be calculated as shown:

Front Porch = (92 pixels) * (27.85ns/pixel) = 2.56E-6 sec.

Back Porch = (180 pixels) * (27.85ns/pixel) = 5.01E-6 sec.

Horizontal sync width = (112 pixels) * (27.85ns/pixel) = 3.12E-6 sec.

Horizontal scan time = (1024 + 92 + 112 + 180)pixels * (27.85ns/pixel) = 39.21E-6 sec. This is equal to 25.50KHz.

3.8 ID/FONT ROM

The Colorcard has an ID/FONT ROM to supply information about the display type and provide initialization information. Additionally, it contains the system FONT. The ROM is a 16K byte wide ROM that is accessed at every other byte as per the FSD Display Rom Definition.

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APPENDIX A

Memory Map

REGISTER	MEMORY ADDRESS
Frame Buffer	$200000 thru $2FFFFF
DIO register 1 (R=ID#/W=reset) (primary=25,sub=1)	$560001 ID = $39
DIO register 3 (R/W)	$560003

bit 0,1,2 = always return 0

bit 3 through 5 = interrupt,with bit 3 equal to LSB of int level

bit 6 = If hi during read then display is requesting an interrupt

bit 7 = Write a one to enable the display for interrupt

ID/FONT ROM	$560005 thru $563FFF(byte addr.)
Topcat registers	$564040 thru $56415E
Nereid registers and color map	$566001 thru $566FFF(byte addr.)

See Pg. 1 for Rest.

APPENDIX B

Clocks and timing registers

Allegro monitor dot clock = 64.1088 MHz.

h1 = $C040
h2 = $1006
h3 = $A008
h4 = $7006
v1 = $C300
v2 = $1003
v3 = $A004
v4 = $7014

Rodan dot clock = 35.904 MHz.

h1 = $C040
h2 = $1008
h3 = $A007
h4 = $7009
v1 = $C190
v2 = $1003
v3 = $A003
v4 = $7013

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0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63											

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SYM	REVISIONS	APPROVED	DATE
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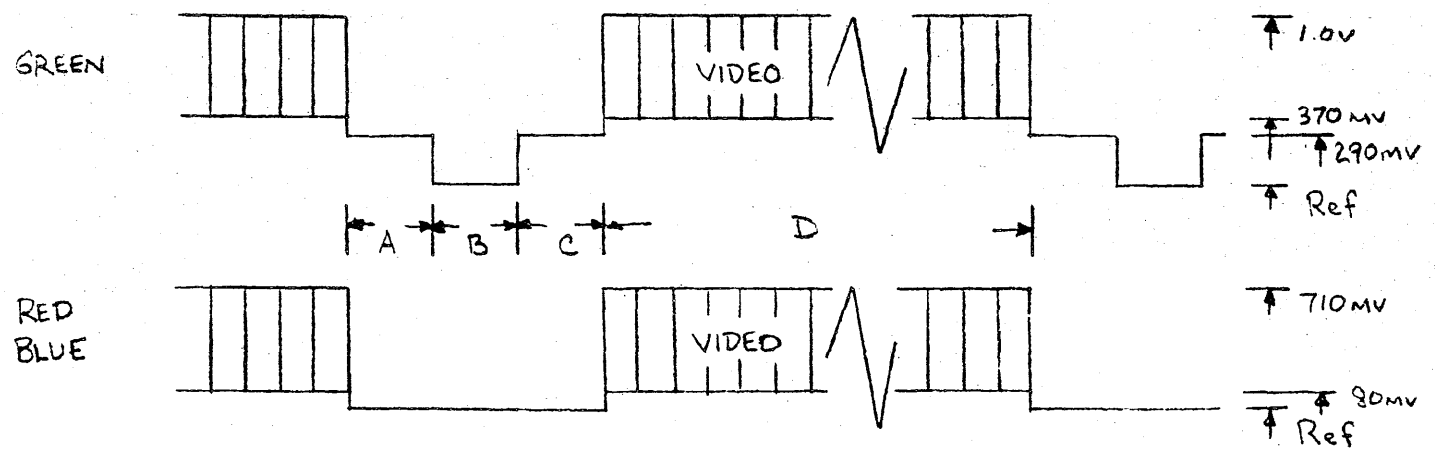
NOTE: Ref may vary from 1 to 2 v.



HORIZONTAL TIME IN μS

	98543	98545
A	2.56	0.935
B	3.12	1.997
C	5.01	2.059
D	28.52	15.97
TOTAL	39.21	20.96

VERTICAL REFRESH RATE = 60HZ with SERRATED SYNC.
HORIZONTAL SCAN RATE = 47.7KHZ (98545A) AND 25.5KHZ (98543A).

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

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